MANOJ KAUSHIK

Physical Design Engineer|STA Engineer mannukaushik1996@gmail.com |
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SUMMARY

- worked at 3rditech IIT Delhi as an STA Engineer (Intern).
- Having 11 months of training experience in a fast-paced environment as an STA/PD Trainee.
- Strong knowledge Digital Electronics and fundamental of CMOS and Fabrication.
- Having sound Knowledge of Static Timing Analysis (STA) Timing Arcs, Delay Models, Setup and Hold time Knowledge of RTL to GDS Flow.
- Good knowledge with files like Netlist, SDC, LIB, LEF, TF, SDF, SPEF.
- Knowledge of scripting language like TCL.
- Hands on experience in Physical Design Flow stages like Synthesis, Floorplan and Power Planning, Placement, CTS, Routing.

EXPERIENCE

- **Company:** 3rditech IIT Delhi
  Position: STA|PD Engineer (Intern/Experience)
  Duration: Oct 2024 –to March 2025

  Contributions:

  - Explored Genus for synthesis, Innovus for PnR, and Tempus for Timing.
  - Proficiency in working on ST40nmand 180nm technology node.
  - Serializer: Digital controller PnR
  - Eight bit counter PnR

- **Training Institute:** |VLSI EXPERT PVT.LTD.(Noida)
  Position: PD/STA Engineer
  Duration: Nov 2023 - Sep 2024
  Key Learning:

  - 11 months of training experience as a STA/PD Trainee.
  - Worked on 32nm and technology nodes.
  - Explored Prime Time for Timing, DC for synthesis, and ICC2 for PnR.

- **University Name: JKLU JAIPUR**

  Position: VLSI Engineer

  Duration: Presently Working.

PROJECTS

- **Physical Design of (Vlsi expert pulp| ICC2) Technology node : 32nm | clock frequency 50MHZ |Instance count :6680 No. of Clock :1**:
  The objective was to create floorplan with different shapes and core utilization, power planning and Placement, analyzing the report for all stages of placement with different floorplan and placement blockages. The final Placement was done with rectangular shape floorplan with aspect ratio of 3:10 and core utilization of 0.6 wire length estimation congestion, , legalization, detailed placement, signoff was aimed with CTS optimization, Routing.

- **Synthesis and Timing optimization of Constrained Design (picorv32a)**:
  The objective was detailed reference Setup for DC and PT. Design, technology and tool specific files were correctly set for complete end to end RTL2GDS flow. The final Placement was done with square shape floorplan with core utilization of0.5, Signoff was aimed with CTS optimization, Routing and timing analysis..

- **Static Timing Analysis of (picorv32a) | Prime Time Technology Node:32nm | Clock Frequency:50MHz | Instance Count:7662 | No. of clocks:1**:
  The objective was to use different library files for different PVT corners and do analysis in single corner Mode, BC WC Mode, OCV Mode by making different TCL scripts for (ff ss, fs sf) timing checks. Learned about the information content of netlist, LIB file, SDC files, SPEF file and there use while doing the timing analysis of the design. Determined the delays for different paths in design and ways to fix the violations in the design like (DRC, ECO, Setup and Hold), delay calculations, GBA and PBA. .

- **Designing of Half and Full Adder using Nand gate | Circuit Simulation**:
  The objective was to design the Schematic of Half and Full Adder using Nand gates.

TECHNICAL SKILLS

- **scripting language TCL**
- **Unix and Linux**
- **Custom Complier(Synopsys)**
- **Prime Time (Synopsys)**

EDUCATION

- **B.TECH Electronic and Communication :** Mar 2013 - Mar 2017
  NIETGreater Noida, UP.
  Percentage:67.60%

- **Intermidiate10+2 :** Mar 2012 - Mar 2013
  B R Memorial SR SEC School Palwal HR
  Percentage:66.8%

- **Matriculation :**
  B R Memorial SR SEC School Palwal HR Nov 2010 - Nov 2011
  Percentage:82.8%

CERTIFICATES

- **Visionsutra Pvt.LTD NewDelhi**:
  One year internshipexperience as Web developer.

LANGUAGES

- English.
- Hindi.